What is claimed is:

1. A circuit for interfacing between a first component operating at a first clock rate and a second component operating at a second clock rate wherein said second clock rate is higher than said first clock rate, said circuit comprising:

a first buffer coupled to said first component;

a second buffer coupled to said second component;

a copy/access controller connected to said first buffer, said second buffer, and said second component and operable to copy data from said first buffer to said second buffer when said first buffer is substantially full, and further operable to prompt said second component to access said second buffer when said data is copied from said first buffer.

2. The circuit as set forth in Claim 1, wherein both said first buffer and said second buffer are random-access memories.

3. The circuit as set forth in Claim 1, wherein both said first buffer and said second buffer are shift registers.

4. The circuit as set forth in Claim 1, wherein said circuit is integrated onto a semiconductor die with one of said first component or said second component.

5. A circuit for transferring a real-time data flow from a first component operable at a first clock rate to a second component operable at a second clock rate wherein said second clock rate is higher than said first clock rate, said circuit comprising:

a first clock signal source of said first clock rate;

a second clock signal source of said second clock rate;

a first buffer operable at either said first clock rate or said second clock rate and coupled to said first component and said second component;

a second buffer operable at either said first clock rate or said second clock rate and coupled to said first component and said second component;

a clock switch coupled to said first buffer and to said second buffer and coupled to said first and second clock signal sources, said clock switch being operable to couple said first clock signal source to either said first buffer or said second buffer and operable to couple said second clock signal source to the other of said first buffer and said second buffer when one of said buffers is substantially full.

6. The circuit as set forth in Claim 5, wherein said circuit is integrated onto the same semiconductor die as one of said first component or said second component.

7. A method for interfacing between a first component operable at a first clock rate and a second component operable at a second clock rate wherein said second clock rate is higher than said first clock rate, comprising the steps of:

transferring data from said first component to a first buffer operable at said first clock rate;

copying data from said first buffer to a second buffer operable at said second clock rate when said first buffer is substantially full; and

prompting said second component to access said data in said second buffer when said copying step is completed.

8. The method as set forth in Claim 7, wherein both said first buffer and said second buffer are shift-register structures.

9. The method as set forth in Claim 7, wherein both said first buffer and said second buffer are random access memories.

10. The method as set forth in Claim 7, wherein said first buffer and said second buffer are both integrated onto the same semiconductor die as one of said first component or said second component.

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